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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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TRINH, MICHAEL MANH

ART UNIT	PAPER NUMBER
2822	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/899,957	Applicant(s) ADKISSON ET AL.	
	Examiner Michael M Trinh	Art Unit 2822	

-- The MAILING DATE of this communication appears on the cover sheet with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 August 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *1-11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

*** This office action is in response to Applicant's election filed on August 12, 2002. Claims 1-22 are currently pending, in which claims 1-11 are non-elected, without traverse.

** Claim 20, line 2, tying error of "processincluding" should be --process including--.

Election/Restrictions

1. Applicant's election filed of Group I, claims 12-22 in Paper No. 5 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors of the given example in the restriction requirement, and because the election is implicitly "without traverse", the election has been treated as an election without traverse (MPEP § 818.03(a)).

2. Claims 1-11 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

4. Claims 12-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Kapoor (5,943,576).

Kapoor teaches an asymmetric field effect transistor comprising: a gate location defined with a trench in a dielectric layer on a semiconductor layer; impurities supplied to the semiconductor layer at edges of the trench and adjacent source and drain regions; a gate structure 419 formed on a semiconductor in the trench, wherein source and drain impurity regions 405,407 adjacent the gate structure 419 (Fig 10A), wherein the insulator or dielectric layer 404 and the

gate structure 419 are planarized (Fig 10A), wherein trench includes sidewall 418. Re further claims 12-21, the claims are directed to the product per se, no matter how actually made by process limitations including "implanting", "diffusion", "angled implantation", "planarizing", "removing", etc..

A "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not.

5. Claims 12-14,17-19,20-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Oyamatsu (5,424229).

Oyamatsu teaches an asymmetric field effect transistor comprising: a gate location defined with a trench in a dielectric layer on a semiconductor layer; impurities supplied to the semiconductor layer at edges of the trench and adjacent source and drain regions (Figs 4B-4D; col 4-5); a gate structure layer 212 formed on a semiconductor in the trench, wherein source and drain impurity regions 214 adjacent the gate structure 213 (Figs 4C-4D), wherein the dielectric layer 204 and the gate structure layer 212 are planarized (Fig 4C; col 5, lines 21-30), wherein trench includes sidewall. As the claims are directed to the product per se, no matter how actually made by process limitations including "implanting", "diffusion" by using a doped material sidewall, "angled implantation", "planarizing", "removing", etc..

A "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the

patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

> This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

7. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over either Kapoor (5,943,576) or Oyamatsu (5,424,229), taken with Hsu (6,291,325).

Kapoor teaches an asymmetric field effect transistor formed on a semiconductor substrate as applied to claims 12-21 above. Oyamatsu teaches an asymmetric field effect transistor formed on a semiconductor substrate as applied to claims 12-14,17-19,20-21 above.

Re claim 22, Kapoor or Oyamatsu lacks to form the transistor on an silicon on insulator (SOI) substrate.

However, Hsu teaches (at col 4, lines 33-46; Figs 10,12,1-3) to alternatively form an asymmetric field effect transistor either on a bulk semiconductor substrate or on a Silicon on Insulator substrate (SOI).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to alternatively form the transistor of Kapoor or Oyamatsu on either the bulk semiconductor substrate or the SOI substrate as taught by Hsu in order to form a thin film field effect transistor having a thin active layer on the SOI substrate, and to form small size devices.

8. Claims 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oyamatsu (5,424,229) taken with Lee (6,214,677).

Oyamatsu teaches an asymmetric field effect transistor formed on a semiconductor substrate as applied to claims 12-14,17-19,20-21 above.

Re claims 15-16, Oyamatsu lacks to form a planarized insulator layer to the gate structure 213 as shown in Figure 4D.

However, Lee teaches (at col 3, lines 47-68; Figs 1C-1D) that after forming source and drain regions 122, deposit an oxide insulator layer and planarized to form the planarized oxide insulator layer 124 with the gate structure 116a (Fig 1D).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the transistor of Oyamatsu by forming a planarized insulator layer on the gate structure as taught by Lee. This is because of the desirability to form a planar device structure, to protect the underlying structure, and to form an interlayer insulator for subsequent electrical connection.

9. Claims 20-21 are further rejected under 35 U.S.C. 103(a) as being unpatentable over Oyamatsu (5,424,229) taken with Chau et al (5,434,093).

Oyamatsu teaches an asymmetric field effect transistor formed on a semiconductor substrate as applied to claims 12-14,17-19 above.

Re claims 20-21, Oyamatsu teaches to form a doped region 210 by angled implantation, but lacks to form a sidewall of a doped material for diffusing impurities as in claims 20-21.

However, Chau teaches (at col 14, line 60 through col 15, line 30; Figs 5a-5d) to form a doped region 503b by diffusing impurities form a sidewall 510b of a doped material.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the transistor having the doped region of Oyamatsu by diffusing

impurities from the sidewall of a doped material as taught by Chau, because these techniques are alternative and equivalent for substitution in order to the doped region at the edge of the gate structure.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (703) 308-2554. The examiner can normally be reached on M-F from 8:30 Am to 4:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Whitehead Jr Carl can be reached on (703) 308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

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Michael Trinh
Primary Examiner